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(54) System for, and method of, ATM segmentation and re-assembly of cells providing streaming data

(57) Data (e.g. legacy LAN traffic) segmented into packets provide a header and a cell payload for each cell in each packet. The cell payloads are transferred to a region address in a host memory in accordance with determinations by a control memory. When the cell payload is to be transmitted from the host memory, the cell payload for a particular region address is combined with the header stored in the control memory for such address. Streaming data (e.g. voice or video) occurs at a regular rate and is not necessarily broken into packets. The streaming data is segmented to provide cell headers and cell payloads. The cell payloads are then transferred to a host receive FIFO in accordance with a determination by the control memory and are stored in a data sink. Cell payloads from a data source are transferred into a host transmit FIFO at a particular rate and are transferred from the host transmit FIFO preferably at a substantially constant rate higher than the particular rate. These FIFO cell payloads are combined with the headers in the control memory. When the cell payloads in the host transmit FIFO become almost depleted, the transmission of the cell payloads from the host transmit FIFO is skipped to allow the host transmit FIFO to receive additional cell payloads from the data source. The transmit and receive FIFO's respectively maintain cell alignment by providing particular controls with respect to the minimum and maximum number of cell payloads in the FIFO's.

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Description

This invention relates to telecommunications systems for, and methods of, transferring telecommunications information through telephone lines. More particularly, this invention relates to systems for, and methods of, transferring streaming data such as digitally encoded video and voice signals efficiently and reliably through telephone lines.

BACKGROUND OF THE INVENTION

Telephone systems in the United States provide central office for receiving signals from calling telephones within a particular radius such as one (1) to two (2) miles from such central office. The telephone signals from the calling telephone are then transmitted through long distances from such central office. The telephone signals then pass to the receiving telephone through a second central office within a radius of one (1) mile to two (2) miles from a receiving telephone. The telephone signals then pass from the second central office to the receiving telephone.

The telephone signals are transmitted long distance between central offices through optical fibers which have replaced other media previously provided for such purposes. The optical fibers have certain distinctive advantages over the lines previously provided. They allow a significantly increased number of signals from different telephones to be transmitted at the same time through the optical fibers. They pass the digitally-encoded signals with a higher accuracy than other media.

Various systems have been adopted to carry digitally-encoded signals for telephone, video, and data services. One of such systems now being adopted is designated as asynchronous transfer mode (ATM). This system is advantageous because it recognizes that generally signals travel in only one direction at any one time between a calling subscriber and a receiving subscriber. The system preserves bandwidth in the other direction so that a maximum number of different messages can be transmitted in such other direction.

In ATM systems, cells are provided to transmit information between access multiplexers or terminals through central offices. Each of the cells contains headers identifying the calling and receiving stations and also contains a payload providing the information being transmitted and received. The cells pass from the calling telephone through the access multiplex to a first central station. The cells then pass through the first central station and optical fibers to a second central station and then to the receiving access multiplex. During the transfer of the cells to the central stations, the headers may be changed. These changes in the address indicate the path that the cell is following between each pair of central stations to reach the receiving telephone.

In the prior art, to reassemble cells into signals at the access multiplex, the header and the payload in each cell have been transferred to a control memory that processes the header to determine what path it came from so that the signal can be reassembled based upon this path. This has created certain difficulties. For example, it has required the control memory to be relatively large, particularly since the memory receives the header and the payload. It has also caused the transfer to be slow, particularly since the header and the payload have to be processed and the payload is generally twelve times longer than the header.

Co-pending application 08/467,311 (a division of co-pending application 08/299,068 filed August 31, 1994) filed by Bradford C. Lincoln, Douglas M. Brady, David R. Meyer and Warner B. Andrews, Jr. on June 6, 1995, and assigned of record to the assignee of record of this application discloses a system for, and a method of, overcoming the disadvantages discussed in the previous paragraphs as occurring in an ATM system. The system and method disclosed and claimed in application serial No. 08/467,311 minimize the time for processing the cells to update the headers as the cells are transferred through the telephone lines between the calling telephone and the receiving telephone.

In one embodiment of the invention disclosed and claimed in application Serial No. 08/467,311, a header and a payload in a cell are separated for transfer between a cell interface and a host memory. The header is transferred to a control memory. For transfer to the host memory, the control memory initially provides a host-memory region address and the region length. The payload is recorded in such region address. The control memory also provides a second host-memory region address, and length, when the payload length exceeds the payload length in the first region address. For transfer from the host memory to the cell interface, the control memory provides a host memory region address. The cell interface passes the payload from such region address.

The system disclosed and claimed in application Serial No. 08/467,311 processes data which are segmented into packets and in which the packet data is further segmented into cells. As discussed above, the cells are then transferred into region addresses in a host memory buffer. The system disclosed and claimed in application Serial No. 08/467,311 relates primarily to packet data such as is provided for legacy LAN traffic.

In addition to packet data, ATM systems deal with streaming data such as voice and video. This data occurs at a regular rate and is not necessarily segmented into relatively large data units such as packets. Furthermore, the final end point for streaming data may not be the host CPU. Instead, it may be a special audio or video subsystem.

Providing a segmentation and reassembly (SAR) system oriented toward the use of a host memory buffer for streaming data has several disadvantages including the following:

1. The streaming data must be copied into the host memory buffer.
2. Buffer management and communication of buffer information between the host and the SAR system requires computing resources from the host computer.
3. In order to keep the overhead of the host memory buffer to a minimum, the buffer must have a size of several ATM cells. This adds to the latency of the streaming data.
4. Additional memory must be provided for the host buffers.

BRIEF DESCRIPTION OF THE INVENTION

This invention provides a system in which the packet data is transmitted and received as discussed above. In addition, the invention provides a system for, and method of, transmitting and receiving the streaming data. In this invention, the streaming data is transmitted from, and is received, in FIFO's. This minimizes the complexity and cost of the system.

In one embodiment of the invention, data (e.g. legacy LAN traffic) segmented into packets provide a header and a cell payload for each cell in each packet. The cell payloads are transferred to a region address in a host memory in accordance with a determination by a control memory. When the cell payload is to be transmitted from the host memory, the cell payload for a particular region address is combined with the header stored in the control memory for such address.

Streaming data (e.g. voice or video) occurs at a regular rate and is not necessarily broken into packets. Furthermore, the end point for the data may not be the host CPU. In this invention, the streaming data is segmented to provide cell headers and cell payloads. The cell payloads are then transferred to a host receive FIFO in accordance with a determination by the control memory and are stored in a data sink. Cell payloads from a data source are transferred into a host transmit FIFO at a particular rate and are transferred from the host transmit FIFO preferably at a substantially constant rate higher than the particular rate. Such cell payloads are combined with the headers in the control memory.

When the cell payloads in the host transmit FIFO become almost depleted, the transmission of the cell payloads from such other FIFO is skipped to allow such other FIFO to receive additional cell payloads from the data source. The transmit and receive FIFO's respectively maintain cell alignment by providing particular controls with respect to the minimum and maximum number of cell payloads in the FIFO's.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

Figure 1 is a schematic block diagram illustrating on a simplified basis the paths of transferring cells of information in an asynchronous transfer mode between a calling station and a receiving station through an access multiplexer;

Figure 2 is a schematic block diagram on a simplified basis of a system included in the system shown in Figure 1 for transferring cell payloads between a cell interface and a host memory while processing the headers of the cells to control changes in the paths of such transfer;

Figure 3 is a schematic functional diagram showing, in additional detail in block form, the operation of the sub-system shown in Figure 2 when the cell payloads are transferred from the receive cell interface to the host memory;

Figure 4 is a schematic flow chart showing, in additional detail in block form, the operation of the subsystem shown in Figure 2 when the cell payloads are transferred from the host memory to the transmit cell interface;

Figure 5 is a schematic block diagram of a system for processing streaming data by using addresses in FIFO's, instead of a host memory buffer, to transmit and receive streaming data;

Figure 6 is a schematic flow chart showing, in additional detail in block form, the successive steps for transmitting cell payloads of streaming data from a host transmit FIFO in a host; and

Figure 7 is a schematic flow chart showing, in additional detail in block form, the successive steps of receiving cell payloads of streaming data at a host receive FIFO in the host.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 illustrates in block form a system generally indicated at 10 and known in the prior art for transferring signals to and from a pair of telephones (or sources) 12 and 14 respectively through lines 16 and 18 to a common access multiplex 20. The telephone (or source) 12 may illustratively transmit or receive television signals and telephone (voice) signals on a line 16 and the telephone (or source) 14 may illustratively transmit or receive television (video) signals and telephone (voice) signals on a line 18. All signals are digitally encoded. For purposes of simplification, the television (video) signals are shown in Figure 1 as being transferred in solid lines and the telephone (voice) signals are shown in Figure 1 as being transferred in broken lines.

The signals in the lines 16 and 18 pass to the access multiplex 20. The respective digitally-encoded transmit signals are segmented into fixed-length cell payloads and a cell header is added to each cell payload to form a cell. Similarly, received cells are reassembled into the respective receive signals. The headers of the cells are generated in the access multiplex to provide a virtual channel indication and/or a virtual path indication. The header indicates the path which is being

followed to pass the cells to a central office 22. The central office 22 may modify the header again in the cells to identify the path through which the cells are subsequently being transferred. The cells may then be transferred either to a television access 24 or to a telephone access 26 at receiving stations generally indicated at 28 in Figure 1.

Figure 2 illustrates one embodiment of a sub-system disclosed and claimed in application Serial No. 08/467,311. This sub-system is generally indicated at 29 and is enclosed within a box defined by broken lines for use with the access multiplex 20 shown in Figure 1 for providing a controlled transfer of ATM cell payloads between a line 30 from a receive cell interface and a host memory 32. When the cells are transferred from the line 30, the cells pass through a receive FIFO 34. The FIFO 34 constitutes a first-in-first-out memory well known in the art to provide a time buffer. The payload in each cell then passes to a reassembly direct memory access (DMA) stage 36. The header in each cell passes to a reassembly state machine 40 for processing.

The header in each cell is introduced from the reassembly state machine 40 to a control memory 38 which processes the header to provide addresses that indicate where the cell payloads are to be stored in the host memory 32. The addresses are then applied through the reassembly state machine 40 to the reassembly direct memory access (DMA) stage 36 to direct the payload from the FIFO 34 through a host interface 42 to a host or system bus 44. The cells are then transferred in the host memory 32 to the addresses indicated by the control memory 38.

Cells may also be transferred to a transmit cell interface through a line 45 by the sub-system 29 shown in Figure 2. The segmentation state machine 50 reads addresses from the control memory 38 that indicate where cell payloads are stored in the host memory 32. The addresses are then applied by the segmentation state machine 50 to the segmentation direct memory access (DMA) 46 to direct the cell payloads to the transmit FIFO 48. The transmit FIFO 48 may be constructed in a manner similar to the receive FIFO 34. The header is introduced by the control memory 38 to the segmentation state machine 50 for combination in the transmit FIFO 48 with the payload. The recombined cell then passes to the transmit cell interface line 45.

Figure 3 shows a flow chart also shown in application Serial No. 08/467,361. This flow chart shows in additional detail the operation of the sub-system shown in Figure 2 in separating the header and the payload in a cell, reassembling the cell payloads and recording the reassembled payloads in the host memory 32. In the flow chart shown in Figure 3, the cell header is initially read as at 70. The header is used to compute a "connection index" (see block 72) to yield a memory address in a reassembly state. This is indicated as a table 73 designated as "Reassembly State" in the control memory 38. The table 73 contains a plurality of virtual channel connections which are respectively designated as "VCC 1", "VCC 2", "VCC 3", etc.

Each of the virtual channel connections 73 contains a table 75 which provides certain information including the address of a region of the host memory 38, the length of the region in the host memory and the protocol information for the virtual channel connection VCC. Figure 3 schematically shows that the table containing the region address in the host memory 38, the length of the region address and the protocol information for the virtual channel connection VCC are being selected from the virtual channel connection designated as "VCC 2". This is indicated by broken lines at 74 and by the table 75 in Figure 3. It will be appreciated that this is schematic and illustrative and that other VCC's may be selected.

The cell from the line 30 in Figure 2 relating to the receive cell interface is then checked with the protocol information in the VCC 2 virtual channel connection in the table 75 in the control memory 38 as indicated at 76 in Figure 3. If the check indicates that the protocol information in the header and the payload is correct, the region address in the host memory 32 and the length of such region are read from the VCC 2 block in the control memory 38 as indicated at 78 in Figure 3. The region address in the host memory 32 is passed to the reassembly DMA 36 in Figure 2 as indicated at 80. The reassembly DMA 36 is then activated to transfer the cell payload from the receive FIFO 34 in Figure 2 to the host memory 32 as indicated at 82 in Figure 3.

As the successive cell payloads for the VCC 2 table 73 are reassembled in the region, a check is made in each reassembly to determine if the end of the region in the VCC 2 channel connection has been reached. This is indicated at 84 in Figure 3. If the answer is "No", the region address for successive cells is incremented for the successive payloads in the VCC 2 channel connection recorded in the host memory region and the region length is decremented by the same amount. A block 86 in Figure 3 indicates this.

If the end of the region in the VCC 2 table in the control memory 38 has been reached, a "Yes" indication is provided from the block 84. This causes a block 88 to be activated in Figure 3. This block is designated as "Read Free Region". The control memory 38 contains a Free Region Queue indicated at 90 in Figure 3. When the block 88 is activated, it causes the next entry in the Free Region Queue 90 to be selected. For example, when entry 1 in the free region queue has been previously selected, entry 2 in the Free Region Queue 90 is now selected. This is indicated by broken lines 92 extending from the entry 2 in the Free Region Queue 90 to a table 94 in Figure 3.

Entry 2 in the Free Region Queue contains a new address region in the host memory 38 and the length of such region. This information is transferred to the table 75 in place of the information previously recorded in the table. The blocks 78, 80, 82, 84, 86 and 88 are now

operated as discussed above to transfer the payloads in the cells on the line 30 to the regions in the host memory 32. At the end of this region, entry 3 in the Free Region Queue may be selected to provide a new region address in the host memory 32 and the length of such region if the payload has not been completely recorded in the host memory 32. The steps described above are repeated in this manner until all of the payload has been recorded in the host memory 32.

Figure 4 shows a flow chart also shown in co-pending application 08/467,361. Figure 4 shows in additional detail the operation of the sub-system shown in Figure 2 in transferring the cell payloads from the host memory 32, reading the header from the control memory 38 to indicate the ATM path, combining the header and the payload into a cell and transferring the cell to the line 45. In the flow chart shown in Figure 4, a block 100 is provided to determine if a VCC cell has been scheduled for a particular time slot. If a cell has not been scheduled, an idle cell (i.e. no cell recorded in a time slot) is transferred to the line 45 in Figure 2. This is indicated by a line 101 in Figure 4.

If a cell has been scheduled for the particular time slot, the block 100 in Figure 4 selects a virtual channel connection in a table 102 in the control memory 38. This table is designated as "Segmentation State" in Figure 4. As shown in Figure 4, the table 102 contains a plurality of virtual channel connections which are illustratively designated as "VCC 1", "VCC 2", "VCC 3", etc. The virtual channel connection VCC 2 is illustratively shown as being selected in the table 102. This is indicated by broken lines 104. It will be appreciated that any other block could have been chosen. The virtual channel connection VCC 2 illustratively includes a header value (to indicate the path of transfer of the cell), a region address, a region length, protocol information and the position of the next region description in the host memory. This is illustrated at 106 in Figure 2.

The header value and the protocol information in the VCC 2 block are read from the control memory 38 as indicated at 108 and 109 respectively in Figure 4. The header value is then transferred to the transmit FIFO 48 in Figure 2 as indicated at 110 in Figure 4 and the region address and length are read from the VCC 2 virtual channel connection as indicated at 112 in Figure 4. The segmentation DMA 46 in Figure 2 is then set up (see block 114 in Figure 4) and the payload is transferred from the host memory region to the transmit FIFO 48 in Figure 2 (see block 116 in Figure 4). A check is made in each transfer of the payload of successive cell to determine if the region being transferred for the virtual channel connection 106 is at the end of its length. This is indicated at 118 in Figure 4.

If the end of the host region in the VCC 2 virtual channel connection has not been reached as indicated at 120 in Figure 4, the region address at 106 in the control memory is incremented to account for the successive payload transferred to the transmit FIFO 48 and the region length is decremented by the same amount (see block 122). This provides an updated record of the region address being processed in the virtual channel connection VCC 2 and an updated record of the remaining length of the region address to be processed in the virtual channel connection VCC 2.

When the end of the region address in the virtual channel connection VCC 2 has been reached, the address of the next region in the host memory 38 and the length of this region address are read as indicated at 124. This next region address is indicated as "Next" in the table 106 and is indicated in additional detail by a table 128 in Figure 4. The table 128 is designated as a "Region Descriptor" to conform to the designation in the block 124. The table 128 also contains a block designated as "Next". The table 128 is then transferred to the position of the table 106 to replace the information previously in the table 106. The address information transferred from the table 128 to the table 106 is then processed in the blocks 108, 109, 110, 112, 114, 116, 118, 120, 122 and 124 in the same manner as described above. Upon the completion of the processing of the region in the table 106, the "Next" block in the table 106 is processed to determine the subsequent host region address in the host memory 32 and the length of this region address.

Figure 5 is a simplified schematic block diagram of a system for transferring streaming data such as video or voice through a system bus (e.g. the host bus 44) to the segmentation and re-assembly sub-system 29 shown in Figure 2 from a host transmit FIFO 150. The host transmit FIFO 150 receives the streaming data from a data source 152. Figure 5 is also a simplified schematic block diagram of a system for transferring streaming data such as video or voice through the bus 44 from the segmentation and re-assembly sub-system 29 shown in Figure 2 to a host receive FIFO 154. The host receive FIFO 154 then passes the received streaming data to a data sink 156. The FIFO's 150 and 154, the data sink 156 and the data source 152 are shown as being included in a host 158 with the host memory 32 also shown in Figure 2.

Figure 6 shows a flow chart for transmitting streaming data from the host transmit FIFO 150 to the segmentation and re-assembly sub-system 29 shown in Figure 2. As shown in Figure 6, a scheduler 170 determines if a cell should be transmitted from the host transmit FIFO 150 or host memory 32. If a cell has not been scheduled, the scheduler sends a signal on a line 172 to a start line 174 to provide another interrogation of the scheduler 170. If the scheduler has sent a cell, a signal is provided on a line 176. This causes a virtual channel connection (VCC) in the table 102 in the control memory 38 to be selected. This has been previously discussed in connection with Figure 4.

A determination is then made as at 178 as to whether the packet data shown in Figure 4 or the streaming data shown in Figure 5 is being transferred

from the host 158. If the system is not operating in the FIFO mode, a signal is produced as at 180. This causes packet data to be processed as discussed above in connection with Figure 4. This is indicated at 182 in Figure 6. This processing continues until a signal is produced on the line 182 to indicate that the processing of the packet data has been completed.

If an indication is provided as at 184 that the system is operating in the FIFO mode, the binary indication of a constant bit rate skip bit (CBR_SKIP) 185 is read from the control memory 38 as indicated at 187. If the binary indication of this bit is a "1", an indication is provided as at 186. Any transfer of streaming data is then skipped. At the same time, the binary indication of the CBR_SKIP bit is changed from a "1" to a "0" as indicated at 189. This provides for the subsequent transmission of the streaming data from the host transmit FIFO 150 in Figure 5.

If the binary indication of the CBR SKIP bit is "0" as indicated at 188, the ATM header 189 is read from the control memory 38 as indicated at 190. This is the header that was previously provided as at 110 in Figure 4. This header is transferred as at 192. The FIFO address 193 in the control memory 38 corresponding to the ATM header is then read from the control memory 38 as indicated at 194 in Figure 6. This indicates where, in host memory space for the host transmit FIFO 150, the payload for the cell (identified by the ATM header read at 190) is located. The segmentation direct memory access (DMA) 46 in Figure 2 is then set up as indicated at 196 in Figure 6. The payload from the host transmit FIFO 150 is then transferred to the transmit FIFO 48 for combination with the cell header for such payload. This combination occurs in the transmit FIFO 48 in Figure 2. As previously indicated, the cell header for such combination is obtained from the control memory 38 and is introduced from the control memory to the segmentation state machine 50 in Figure 2.

The cell schedule in the segmentation and reassembly sub-system 29 in Figure 2 is set to output the payload from cells from the FIFO 150 at a substantially constant rate. This rate is slightly higher than the fixed rate at which the payload from cells is transferred from the data source 152 into the host transmit FIFO 150. Because of this, the number of cell payloads in the host transmit FIFO 150 becomes progressively depleted. When the depletion reaches a particular value, the host transmit FIFO 150 provides an "almost empty" flag to indicate that there is only a minimal number of cell payloads remaining in the host transmit FIFO 150. For example, the "almost empty" flag may be provided when there is only one (1) cell payload remaining in the host transmit FIFO 150. Alternatively, the flag may be provided when there is only a small number (e.g. 5) cell payloads remaining in the FIFO 150.

When the flag is provided, the CBR_SKIP bit is set to "1". As previously indicated at 186 in Figure 5, the transmission of cell payloads from the FIFO 150 is interrupted when the CBR_SKIP bit has a binary indication of "1". During this interruption, the data source 152 introduces cell payloads to the FIFO 150 to at least partially fill the FIFO. The CBR_SKIP bit is then set to a binary "0" by the segmentation and re-assembly subsystem 29 in Figure 2 to obtain a continuation of the transfer of the cell payloads from the FIFO 150 to the segmentation direct memory access (DMA) stage 46 in Figure 2.

Figure 7 shows a flow chart for transmitting payloads relating to streaming data to the host receive FIFO 154 in Figure 5 from the segmentation and reassembly (SAR) sub-system 29 in Figure 2. As a first step, an interrogation is made to determine if there is an ATM header match. For example, this interrogation may be made to determine if the header for each cell from the receive cell interface 30 in Figure 2 is in proper form. This is indicated at 200 in Figure 7. If the answer is "no" as indicated at 201, the interrogation is made again. If the answer is "yes" as indicated at 202 in Figure 7, one of the virtual channel connections (VCC) 73 (also shown in Figure 3) in the control memory 38 is selected. This is indicated at 204 in Figure 7.

As indicated at 206 in Figure 7, a determination is then made of the FIFO mode 207 in the control memory 38 as to whether the cells relate to the FIFO mode. If the answer is "no" as indicated at 208, a virtual control connection (VCC) 73 in the control memory 38 relating to packet data is processed. This processing is indicated at 210 in Figure 7. The processing is indicated in Figure 3 and is discussed above in connection with the showing in Figure 3. The processing provides for the transfer of cell payloads into the host memory 32 in Figure 2. If a determination is made as indicated at 212 in Figure 7 that the cells being transferred relate to the FIFO mode, the FIFO address 213 in the control memory 38 of the host receive FIFO 154 in the control memory 38 is read as indicated at 214 in Figure 7. Such reading is indicated in the flow chart at 216 in Figure 7.

The address of the host receive FIFO 154 is determined in the control memory 38 as discussed above in connection with Figures 2 and 3. The address of the host receive FIFO 154 is then introduced to the reassembly state machine 40 in Figure 2 and is combined in the re-assembly DMA 36 with the cell payload from the receive FIFO 34. The numeral 218 in Figure 7 indicates this combination. The cell payload is then transferred to the host receive FIFO 154 in accordance with the address in the reassembly direct memory access 36. This is indicated at 220 in Figure 7. This transfer occurs through the system bus 44.

A transfer of cell payloads from the FIFO 150 or to the FIFO 154 may be interrupted as a result of activity on the system bus 44 with a higher priority than such FIFO transfers. When the transfer from the host transmit FIFO 150 or to the host receive FIFO 154 resumes, the address of the FIFO on the system bus 44 will be the original FIFO address plus the number of bytes trans-

ferred from the host transmit FIFO 150 or to the host receive FIFO 154 before the interruption. For this reason, the address decode for both the host transmit FIFO 150 and the host receive FIFO 154 should respond to a range of addresses including the original FIFO address plus forty eight (48). The numeral forty eight (48) represents the number of bytes in an ATM cell payload.

Both the host transmit FIFO 150 and the host receive FIFO 154 should insure that they maintain cell alignment. The host transmit FIFO 150 maintains cell alignment by transferring a cell payload only when there is at least one (1) complete cell (or any specified number of cells other than one (1)) at the start of a transfer from the address in the FIFO. The host receive FIFO 154 maintains cell alignment by storing a cell payload only when there is room in the FIFO to receive at least one (1) complete cell payload at the beginning of an address from the FIFO.

The system and method disclosed above have certain important advantages. They provide for the segmentation and re-assembly of both packet data and streaming data. In providing such segmentation and reassembly, the system and method of this invention provide for the segmentation of the cell header from the cell payload and the processing of the cell in the control memory 38 to provide a correlation between the cell header and the address of the cell payload in the host. In the case of packet data, the cell payload is transferred to or from a region address in the host memory 32 in the host. In the case of streaming data, the cell payload is transferred to the host transmit FIFO 150 or from the host receive FIFO 154. By employing the host FIFO's 150 and 154 for the streaming data instead of the host memory 32, the operation of the host memory 32 is significantly simplified, and the size and cost of the host memory is considerably reduced, in comparison to the cost and complexity of adding the host FIFO's 150 and 154.

Although this invention has been disclosed and illustrated with reference to particular embodiments, the principles involved are susceptible for use in numerous other embodiments which will be apparent to persons of ordinary skill in the art. The invention is, therefore, to be limited only as indicated by the scope of the appended claims.

According to its broadest aspect the invention provides in a combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a payload constituting streaming data such as voice or video, a FIFO, first means for receiving the cells, second means for transferring the headers in the cells, third means for transferring the payload in the cells, and control memory means.

It should be noted that the objects and advantages of the invention may be attained by means of any compatible combination(s) particularly pointed out in the items of the following summary of the invention and the appended claims.

SUMMARY OF THE INVENTION

1. In combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a payload constituting streaming data such as voice or video,

a FIFO,
first means for receiving the cells,
second means for transferring the headers in the cells,
third means for transferring the payload in the cells,
control memory means responsive to the headers transferred by the second means for providing an address in the FIFO where the separated payload is to be transferred, and
fourth means responsive to the address provided in the FIFO by the control memory means and to the payload from the third means for transferring the payload in the cells to the selected region address in the FIFO identified by the control memory means.

2. In a combination

fifth means for remembering the address of the FIFO transferring the streaming data at each instant in case of an interruption in the transfer of such streaming data to the FIFO, and
sixth means for resuming the transfer of such streaming data to the FIFO at the address remembered by such FIFO at the time of the interruption in the transfer of such streaming data to the FIFO.

3. In a combination

fifth means for providing in the control memory means a state table entry containing the header in the control memory means for such streaming data, the address of the FIFO and an indication of whether streaming data is to be provided, and
sixth means for providing for the transfer of the streaming data to the address in the FIFO in accordance with the indication that the streaming data is to be transmitted.

4. In a combination

fifth means for updating the region address in the FIFO upon each transfer of the payload in the cell by the fourth means to the FIFO.

5. In a combination

fifth means for updating the region address in the control memory means upon each transfer of the payload in the cell by the fourth means to the FIFO.

6. In a combination

host memory means having region addresses, the control memory means being responsive to packet data and to the headers transferred by the second means for selecting the region address in the host memory means for recording the payload in the host memory means, and fifth means responsive to the region address selected in the host memory means by the control memory means and to the payload from the third means for transferring the payload in the cells to the selected region address in the host memory means.

7. In a combination

means for updating the address in the control memory means upon each transfer of the cell payload to one of the addresses in the FIFO, and
means for transferring the payload to each successive one of the different addresses identified in the FIFO means by the address in the control memory means upon each transfer of the payload to a previous one of the different addresses identified in the FIFO means by the address in the control memory means.

8. In a combination

means for transferring the cell payload to each individual one of the different addresses identified in the FIFO by the address in the control memory means upon each transfer of the payload to a previous one of the addresses identified in the FIFO by the address in the control memory means.

9. In combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a streaming data payload such or voice or video,

control memory means providing a first address,
a FIFO having a plurality of addresses for receiving, storing and transferring the cell payload,
interface means,
state machine means responsive to the cell for separating the payload in the cell and the header in the cell,
the control memory means being responsive to the cell headers for providing for the transfer of the cell payload between the individual one of the addresses identified in the FIFO by the address in the control memory means bind the interface means, and
payload transfer means for transferring the cell payload between the individual ones of the addresses identified in the FIFO by the address in the control memory means and the interface means.

10. In a combination

means for identifying whether the transfer of the payload is to be made to the FIFO through the interface means, and
means for providing for the transfer of the payload to the FIFO through the interface means only when the transfer of the payload is identified to be made to the FIFO.

11. In a combination

means for providing in the control memory means a state table entry containing the header in the control memory means for such streaming data, the address of the FIFO and an indication that the payload constitutes streaming data, and
means from transferring the streaming data to the FIFO through the interface means at the addresses specified for the FIFO in the state table entry.

12. In a combination

means for identifying whether the transfer of the payload is to be made from the FIFO through the interface means, and
means for providing for the transfer of the payload from the FIFO through the interface means only when the transfer of the payload is identified to be made from the FIFO.

13. In a combination

means for providing in the state table entry an indication of whether the transfer of the payload into the addresses in the FIFO is to be provided or skipped, and
means for transferring or skipping the transfer of the payload from the FIFO in accordance with the indication provided by the last mentioned means.

14. In a combination

host memory means having a plurality of addresses for receiving, storing and transferring the cell payload,

the control memory means providing a first region address for packet data and being responsive to the cell headers for packet data for providing for the transfer of the cell payload between the individual one of the addresses identified in the host memory means by the first region address in the host memory means and the interface means and

means for transferring the cell payload for packet data between the individual ones of the region addresses identified in the host memory means by the control memory means and the interface means.

15. In combination for providing in an asynchronous transfer mode (ATM) cells which have headers providing addresses and having a payload providing streaming data such as voice or video,

a FIFO having a plurality of different addresses for receiving, storing and transferring the payload in the cell,

interface means,

means for transferring the payload in the cells from an individual one of the FIFO and the interface means to the other one of the FIFO and the interface means,

a state machine for separating the cell headers and the payload in the cells,

control memory means responsive to the header from the state machine for modifying the header in accordance with the direction of the transfer of the cell from the individual one of the FIFO and the interface means to the other one of the FIFO and the interface means, and

means responsive to the modified header from the control memory means for transferring the payload from the individual one of the FIFO and the interface means to the other one of the FIFO and the interface means.

16. In a combination

the control memory means indicating an address in the FIFO, the address identifying a number of the different addresses in the FIFO, and

means for transferring the payload between the successive ones of the different addresses in the FIFO and the interface means in response to the modified header from the control memory means.

17. In a combination

the control memory means being operative to provide the address in the header when the cell payload is being transferred to the interface means from the addresses identified in the FIFO by the address in the control memory means.

18. In a combination

means for maintaining cell alignment in the transfer of the payload to the interface means from the address as identified in the FIFO by the address in the control memory means.

19. In a combination

means for maintaining cell alignment in the transfer of the payload from the individual one of the FIFO and the interface means to the other one of the FIFO and the interface.

20. In a combination

the control memory means being operative to include the region address in the FIFO when the payload is being transferred to the FIFO from the interface means.

21. In a combination

means for maintaining cell alignment in the transfer of the payload to the FIFO from the interface means.

22. In combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a payload constituting streaming data such as voice or video,

a FIFO having a plurality of addresses for receiving, storing and transferring the payload in the cell,

interface means,

means for providing the cell payload at the interface means,

a state machine for separating the cell headers and the cell payload,

control memory means responsive to the cell header from the state machine for modifying the cell header to indicate a region address in which the cell payload is to be recorded in the FIFO, the address including a number of the different addresses in the FIFO, and

means for transferring the payload to the addresses identified in the FIFO by the addresses in the control memory means in accordance with the modified cell headers.

23. In a combination

means for counting the number of the FIFO addresses receiving the payload, and
means for resuming the transfer of the payload to the FIFO, after any interruption in such transfer, in accordance with the counted number of the FIFO addresses receiving the payload.

24. In a combination

means for maintaining cell alignment in the FIFO by transferring data into the FIFO only when the FIFO has room for receiving at least one complete cell at the beginning of a transfer to the FIFO address.

25. In a method of providing in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a payload constituting streaming data such as voice or video, the steps of:

providing interface means,
providing a FIFO having a plurality of addresses for receiving, storing and transferring the cell payload,
separating the cell header and the cell payload,
providing a control memory,
modifying the cell header in the control memory in accordance with the direction of transfer of the cell from the individual one of the interface means and the FIFO to the other one of the interface means and the FIFO, and
transferring the cell payload from the individual one of the interface means and the FIFO to the other one of the interface means and the FIFO in accordance with the modified header.

26. In a method wherein

the cell payload is transferred from a data source to the FIFO at a first rate and is transferred from the FIFO to the interface means at a second rate higher than the first rate.

27. In a method wherein the transfer of the cell payload from the FIFO to the interface means is skipped when a particular number of cells remain in the FIFO, thereby giving the FIFO an opportunity during such skipping to become at least partially filled with additional cells transferred from the data source.

28. In a method wherein

cell alignment is maintained in the FIFO by transferring the cell payload from the FIFO to the interface means only when there is at least one complete cell in the FIFO at the beginning of a transfer from the FIFO address.

29. In a method wherein

the address of the FIFO is read from the control memory and wherein the address of the FIFO and the cell payload are combined and the combination is transferred to the FIFO from the interface means.

30. In a method the steps of:

providing a host memory having a plurality of addresses for receiving, storing and transferring the cell payload for packets of data, and
transferring the cell payload for the packets of data from the individual one of the interface means and the host memory means to the other one of the interface means and the host memory means in accordance with the modified header.

31. In a method the steps of:

providing a host memory having a plurality of addresses for receiving, storing and transferring the cell payload for packets of data, and
transferring the cell payload for the packets of data from the host memory means to the interface means in accordance with the modified header.

32. In a method the steps of:

providing a host memory having a plurality of addresses for receiving, storing and transferring the cell payload for packets of data, and
transferring the cell payload for the packets of data from the interface means to the host memory means in accordance with the modified header.

33. In a method wherein

cell alignment is maintained in the FIFO by transferring the cell payload from the interface means to the FIFO only when there is room in the FIFO for at least one cell to be transferred to the FIFO at the start of a transfer of the cell payloads to the FIFO.

34. In combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a payload constituting streaming data such as voice or video,

a FIFO having a plurality of different addresses

for receiving, storing and transferring the payload,

a control memory for storing the cell headers for the cell payload and for storing the addresses provided in the FIFO for the cell payload,

state machine means for processing an individual one of the header provided in the cell for the cell payload and the addresses provided in the FIFO for the cell payload depending upon the transfer of the cell payload to or from the FIFO, and

means for combining the cell payloads and the individual ones of the headers provided for the cell payload and the addresses provided in the FIFO for the cell payload depending upon the transfer of the cell payload to or from the FIFO.

35. In a combination wherein

the FIFO includes a number of the addresses identified in an address in the control memory and wherein

the state machine means provides for the transfer of the cell payload to or from the different addresses identified in the FIFO by the address in the control memory depending upon the transfer of the cell payload to or from the FIFO.

36. In a combination wherein

the address provided in the control memory for the addresses in the FIFO, includes the number of the addresses in the FIFO and wherein

the state machine means keeps account of the number of the cell payloads transferred from the FIFO in relation to the number of the addresses provided in the control memory for the FIFO.

37. In combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which having a payload constituting streaming data such as voice and video,

a FIFO having a plurality of different addresses for receiving, storing and transferring the cell payload,

first means for providing a transfer of the cell payload,

a control memory for providing an address indicating a number of the different addresses in the FIFO and for storing the cell header and for providing the header, and

state machine means for providing for the transfer of the cell payload between the different addresses identified in the FIFO by the address in the control memory and the first means in accordance with a selective one of the addresses in the FIFO and the cell header in the control memory.

38. In a combination wherein

the state machine means provides a selection between the cell header and the address in the control memory to receive the cell payload and wherein

the first means combines the cell payload and the selected one of the header in the cell and the address in the control memory.

39. In a combination wherein

the state machine means combines the header in the cell and the cell payload during the transfer of the cell payload from the FIFO.

40. In a combination wherein

the state machine means combines the address in the control memory and the cell payload during the transfer of the cell payload to the FIFO.

Claims

1. In combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a payload constituting streaming data such as voice or video,

a FIFO,

first means for receiving the cells,

second means for transferring the headers in the cells,

third means for transferring the payload in the cells,

control memory means responsive to the headers transferred by the second means for providing an address in the FIFO where the separated payload is to be transferred, and

fourth means responsive to the address provided in the FIFO by the control memory means and to the payload from the third means for transferring the payload in the cells to the selected region address in the FIFO identified by the control memory means.

2. In a combination as set forth in claim 1,

fifth means for remembering the address of the

FIFO transferring the streaming data at each instant in case of an interruption in the transfer of such streaming data to the FIFO, and

sixth means for resuming the transfer of such streaming data to the FIFO at the address remembered by such FIFO at the time of the interruption in the transfer of such streaming data to the FIFO,

and/or further preferably comprising

fifth means for providing in the control memory means a state table entry containing the header in the control memory means for such streaming data, the address of the FIFO and an indication of whether streaming data is to be provided, and

sixth means for providing for the transfer of the streaming data to the address in the FIFO in accordance with the indication that the streaming data is to be transmitted,

and/or further preferably comprising

fifth means for updating the region address in the FIFO upon each transfer of the payload in the cell by the fourth means to the FIFO,

and/or further preferably comprising

fifth means for updating the region address in the control memory means upon each transfer of the payload in the cell by the fourth means to the FIFO,

and/or further preferably comprising

host memory means having region addresses, the control memory means being responsive to packet data and to the headers transferred by the second means for selecting the region address in the host memory means for recording the payload in the host memory means, and

fifth means responsive to the region address selected in the host memory means by the control memory means and to the payload from the third means for transferring the payload in the cells to the selected region address in the host memory means,

and/or further preferably comprising

means for updating the address in the control memory means upon each transfer of the cell payload to one of the addresses in the FIFO, and

means for transferring the payload to each successive one of the different addresses identified in the FIFO means by the address in the control memory means upon each transfer of the payload to a previous one of the different addresses identified in the FIFO means by the address in the control memory means,

and/or further preferably comprising

means for transferring the cell payload to each individual one of the different addresses identified in the FIFO by the address in the control memory means upon each transfer of the payload to a previous one of the addresses identified in the FIFO by the address in the control memory means.

3. In combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a streaming data payload such or voice or video,

control memory means providing a first address,

a FIFO having a plurality of addresses for receiving, storing and transferring the cell payload,

interface means,

state machine means responsive to the cell for separating the payload in the cell and the header in the cell,

the control memory means being responsive to the cell headers for providing for the transfer of the cell payload between the individual one of the addresses identified in the FIFO by the address in the control memory means and the interface means, and

payload transfer means for transferring the cell payload between the individual ones of the addresses identified in the FIFO by the address in the control memory means and the interface means.

4. In a combination as set forth in any of the preceding claims, means for identifying whether the transfer of the payload is to be made to the FIFO through the interface means, and

means for providing for the transfer of the payload to the FIFO through the interface means only when the transfer of the payload is identified to be made to the FIFO,

and/or further preferably comprising

means for providing in the control memory means a state table entry containing the header in the control memory means for such streaming data, the address of the FIFO and an indication that the payload constitutes streaming data, and

means from transferring the streaming data to the FIFO through the interface means at the addresses specified for the FIFO in the state table entry,

and/or further preferably comprising

means for identifying whether the transfer of the payload is to be made from the FIFO through the interface means, and

means for providing for the transfer of the payload from the FIFO through the interface means only when the transfer of the payload is identified to be made from the FIFO,

and/or further preferably comprising

means for providing in the state table entry an indication of whether the transfer of the payload into the addresses in the FIFO is to be provided or skipped, and

means for transferring or skipping the transfer of the payload from the FIFO in accordance with the indication provided by the last mentioned means,

and/or further preferably comprising

host memory means having a plurality of addresses for receiving, storing and transferring the cell payload,

the control memory means providing a first region address for packet data and being responsive to the cell headers for packet data for providing for the transfer of the cell payload between the individual one of the addresses identified in the host memory means by the first region address in the host memory means and the interface means and

means for transferring the cell payload for packet data between the individual ones of the region addresses identified in the host memory means by the control memory means and the interface means.

5. In combination for providing in an asynchronous transfer mode (ATM) cells which have headers providing addresses and having a payload providing streaming data such as voice or video,

a FIFO having a plurality of different addresses for receiving, storing and transferring the payload in the cell,

interface means,

means for transferring the payload in the cells from an individual one of the FIFO and the interface means to the other one of the FIFO and the interface means,

a state machine for separating the cell headers and the payload in the cells,

control memory means responsive to the header from the state machine for modifying the header in accordance with the direction of the transfer of the cell from the individual one of the FIFO and the interface means to the other one of the FIFO and the interface means, and

means responsive to the modified header from the control memory means for transferring the payload from the individual one of the FIFO and the interface means to the other one of the FIFO and the interface means.

6. In a combination as set forth in any of the preceding claims, the control memory means indicating an address in the FIFO, the address identifying a number of the different addresses in the FIFO, and

means for transferring the payload between the successive ones of the different addresses in the FIFO and the interface means in response to the modified header from the control memory means,

and/or further preferably comprising

the control memory means being operative to provide the address in the header when the cell payload is being transferred to the interface means from the addresses identified in the FIFO by the address in the control memory means,

and/or further preferably comprising

means for maintaining cell alignment in the transfer of the payload to the interface means from the address as identified in the FIFO by the address in the control memory means,

and/or further preferably comprising

means for maintaining cell alignment in the transfer of the payload from the individual one of the FIFO and the interface means to the other one of the FIFO and the interfaces,

and/or further preferably comprising

the control memory means being operative to include the region address in the FIFO when the payload is being transferred to the FIFO from the interface means,

and/or further preferably comprising

means for maintaining cell alignment in the transfer of the payload to the FIFO from the interface means.

7. In combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a payload constituting streaming data such as voice or video,

a FIFO having a plurality of addresses for receiving, storing and transferring the payload in the cell,

interface means,

means for providing the cell payload at the interface means,

a state machine for separating the cell headers and the cell payload,

control memory means responsive to the cell header from the state machine for modifying the cell header to indicate a region address in which the cell payload is to be recorded in the FIFO, the address including a number of the different addresses in the FIFO, and

means for transferring the payload to the addresses identified in the FIFO by the addresses in the control memory means in accordance with the modified cell headers.

8. In a combination as set forth in any of the preceding claims, means for counting the number of the FIFO

addresses receiving the playload, and

means for resuming the transfer of the payload to the FIFO, after any interruption in such transfer, in accordance with the counted number of the FIFO addresses receiving the payload,

and/or further preferably comprising

means for maintaining cell alignment in the FIFO by transferring data into the FIFO only when the FIFO has room for receiving at least one complete cell at the beginning of a transfer to the FIFO address.

9. In a method of providing in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a payload constituting streaming data such as voice or video, the steps of:

providing interface means,
providing a FIFO having a plurality of addresses for receiving, storing and transferring the cell payload,
separating the cell header and the cell payload,
providing a control memory,
modifying the cell header in the control memory in accordance with the direction of transfer of the cell from the individual one of the interface means and the FIFO to the other one of the interface means and the FIFO, and
transferring the cell payload from the individual one of the interface means and the FIFO to the other one of the interface means and the FIFO in accordance with the modified header.

10. In a method as set forth in any of the preceding claims wherein the cell payload is transferred from a data source to the FIFO at a first rate and is transferred from the FIFO to the interface means at a second rate higher than the first rate,

and/or wherein preferably

the transfer of the cell payload from the FIFO to the interface means is skipped when a particular number of cells remain in the FIFO, thereby giving the FIFO an opportunity during such skipping to become at least partially filled with additional cells transferred from the data source,

and/or wherein preferably

cell alignment is maintained in the FIFO by transferring the cell payload from the FIFO to the interface means only when there is at least one complete cell in the FIFO at the beginning of a transfer from the FIFO address,

and/or wherein preferably

the address of the FIFO is read from the control memory and wherein the address of the FIFO and the cell payload are combined and the combination is transferred to the FIFO from the interface means,

and/or further preferably comprising the steps of:

providing a host memory having a plurality of addresses for receiving, storing and transferring the cell payload for packets of data, and
transferring the cell payload for the packets of data from the individual one of the interface means and the host memory means to the other one of the interface means and the host memory means in accordance with the modified header,

and/or further preferably comprising the steps of:

providing a host memory having a plurality of addresses for receiving, storing and transferring the cell payload for packets of data, and
transferring the cell payload for the packets of data from the host memory means to the interface means in accordance with the modified header,

and/or further preferably comprising the steps of:

providing a host memory having a plurality of addresses for receiving, storing and transferring the cell payload for packets of data, and
transferring the cell payload for the packets of data from the interface means to the host memory means in accordance with the modified header,

and/or wherein preferably

cell alignment is maintained in the FIFO by transferring the cell payload from the interface means to the FIFO only when there is room in the FIFO for at least one cell to be transferred to the FIFO at the start of a transfer of the cell payloads to the FIFO.

11. In combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a payload constituting streaming data such as voice or video,

a FIFO having a plurality of different addresses for receiving, storing and transferring the payload,
a control memory for storing the cell headers for the cell payload and for storing the addresses provided in the FIFO for the cell payload,
state machine means for processing an individual one of the header provided in the cell for the cell payload and the addresses provided in the FIFO for the cell payload depending upon the transfer of the cell payload to or from the FIFO, and
means for combining the cell payloads and the

individual ones of the headers provided for the cell payload and the addresses provided in the FIFO for the cell payload depending upon the transfer of the cell payload to or from the FIFO.

12. In a combination as set forth in any of the preceding claims wherein

the FIFO includes a number of the addresses identified in an address in the control memory and wherein
the state machine means provides for the transfer of the cell payload to or from the different addresses identified in the FIFO by the address in the control memory depending upon the transfer of the cell payload to or from the FIFO, and/or wherein preferably
the address provided in the control memory for the addresses in the FIFO, includes the number of the addresses in the FIFO and wherein
the state machine means keeps account of the number of the cell payloads transferred from the FIFO in relation to the number of the addresses provided in the control memory for the FIFO.

13. In combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which having a payload constituting streaming data such as voice and video,

a FIFO having a plurality of different addresses for receiving, storing and transferring the cell payload,
first means for providing a transfer of the cell payload,
a control memory for providing an address indicating a number of the different addresses in the FIFO and for storing the cell header and for providing the header, and
state machine means for providing for the transfer of the cell payload between the different addresses identified in the FIFO by the address in the control memory and the first means in accordance with a selective one of the addresses in the FIFO and the cell header in the control memory.

14. In a combination as set forth in any of the preceding claims wherein

the state machine means provides a selection between the cell header and the address in the control memory to receive the cell payload and wherein
the first means combines the cell payload and the selected one of the header in the cell and the address in the control memory,
and/or wherein preferably
the state machine means combines the header in the cell and the cell payload during the transfer of the cell payload from the FIFO,
and/or wherein preferably
the state machine means combines the address in the control memory and the cell payload during the transfer of the cell payload to the FIFO.

15. In a combination for transferring in an asynchronous transfer mode (ATM) cells which have headers providing addresses and which have a payload constituting streaming data such as voice or video,

a FIFO,
first means for receiving the cells,
second means for transferring the headers in the cells,
third means for transferrring the payload in the cells, and
control memory means.

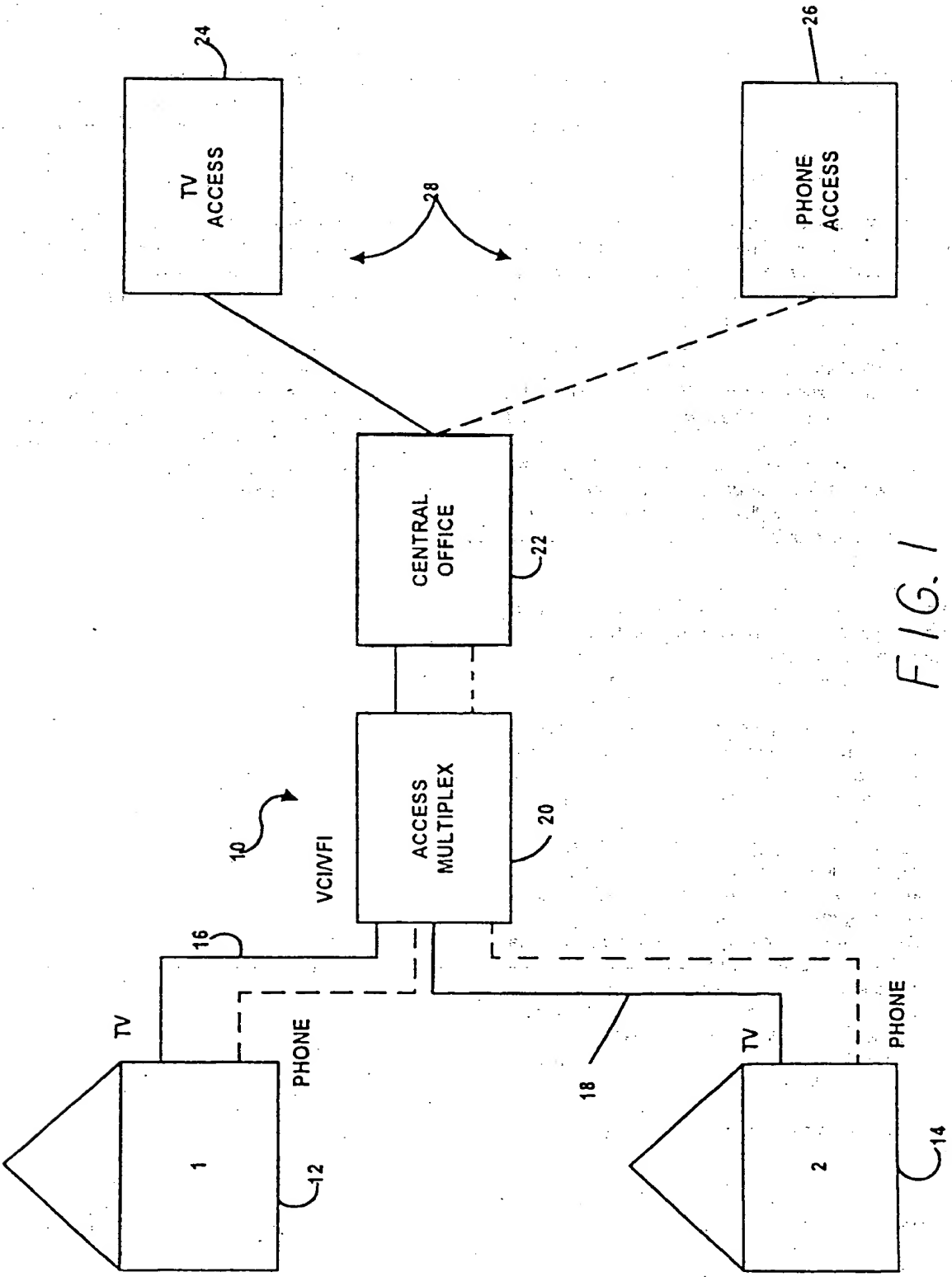

FIG. 1

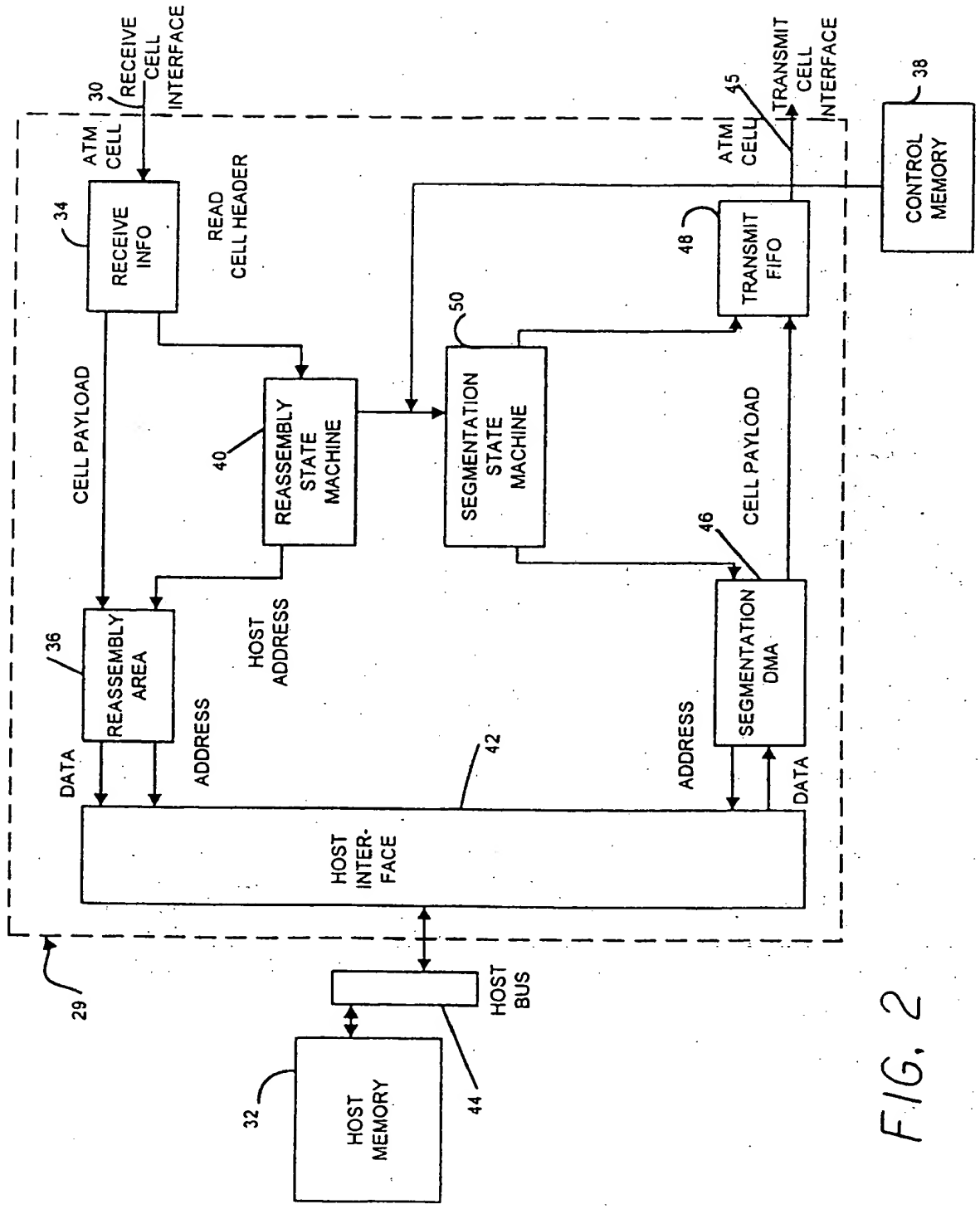
RECEIVE CELL INTERFACE
30
ATM CELL
RECEIVE INFO
34
READ CELL HEADER
CELL PAYLOAD
REASSEMBLY STATE MACHINE
40
REASSEMBLY AREA
36
HOST ADDRESS
ADDRESS
DATA
HOST INTER-FACE
42
29
HOST BUS
44
HOST MEMORY
32
SEGMENTATION STATE MACHINE
50
TRANSMIT FIFO
48
ATM CELL
45
TRANSMIT CELL INTERFACE
CONTROL MEMORY
38
CELL PAYLOAD
SEGMENTATION DMA
46
ADDRESS
DATA

FIG. 2

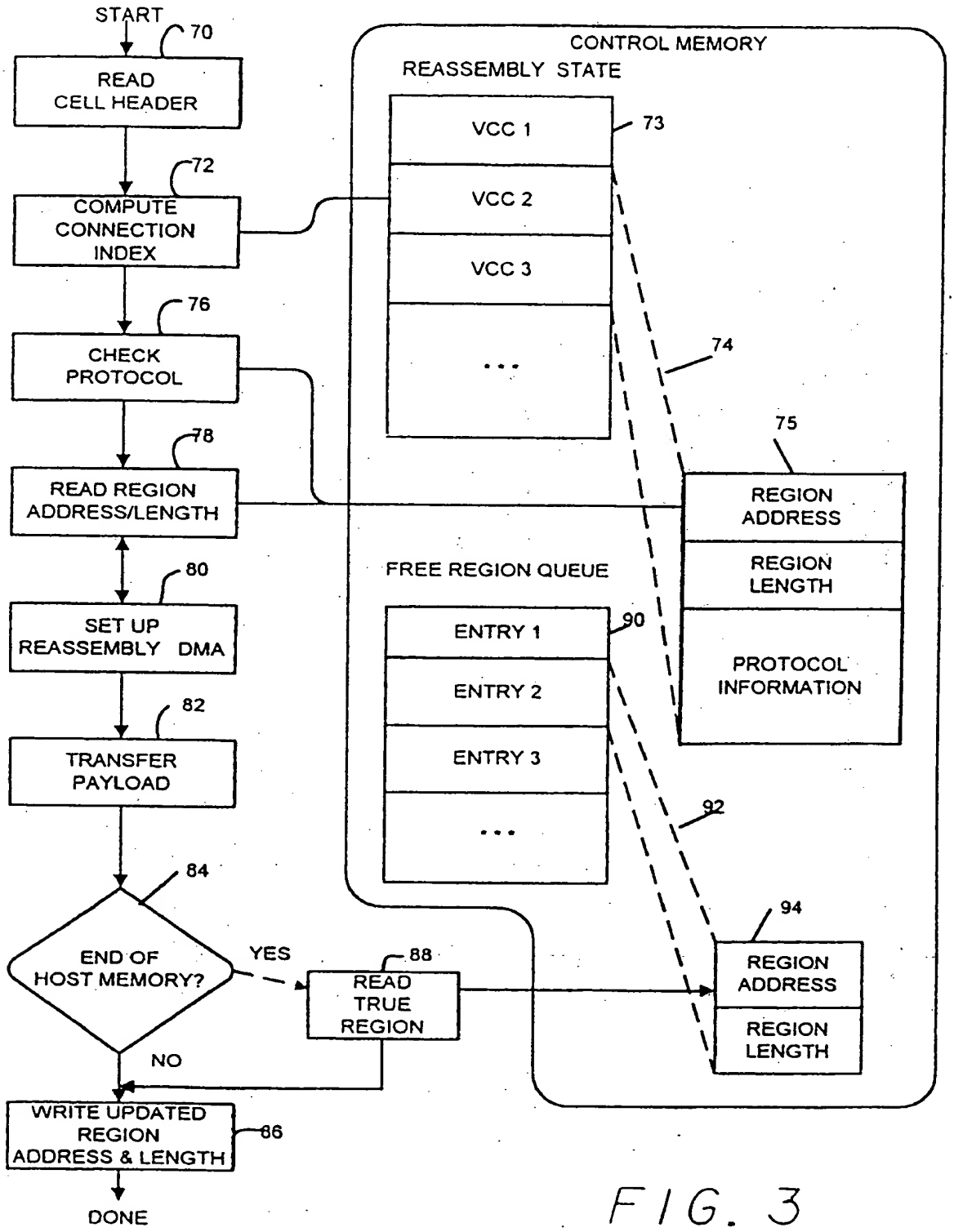

FIG. 3

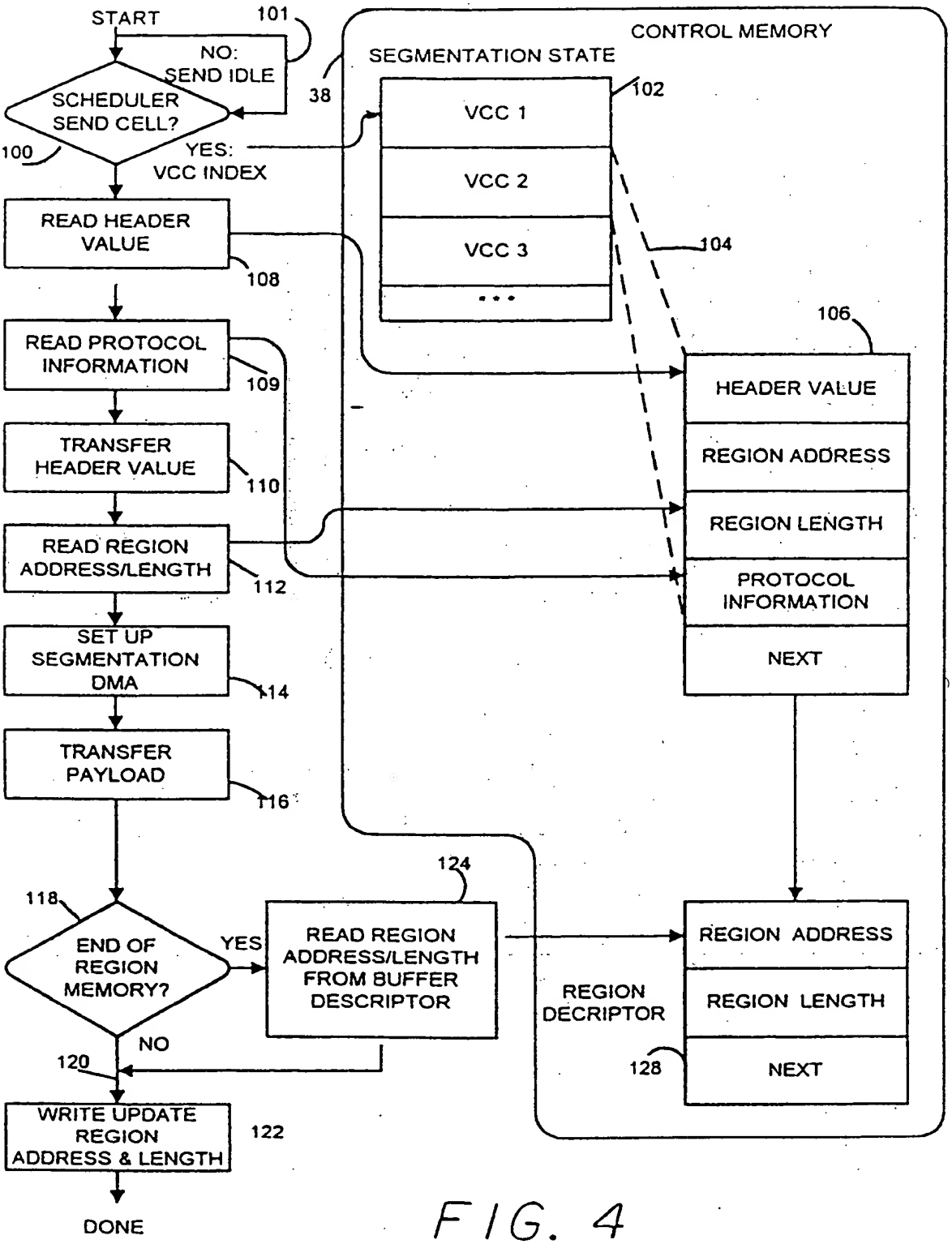
START
101
NO: SEND IDLE
SCHEDULER SEND CELL?
100
YES: VCC INDEX
READ HEADER VALUE
108
READ PROTOCOL INFORMATION
109
TRANSFER HEADER VALUE
110
READ REGION ADDRESS/LENGTH
112
SET UP SEGMENTATION DMA
114
TRANSFER PAYLOAD
116
118
END OF REGION MEMORY?
YES
NO
120
WRITE UPDATE REGION ADDRESS & LENGTH
122
DONE
CONTROL MEMORY
SEGMENTATION STATE
38
VCC 1
VCC 2
VCC 3
102
104
106
HEADER VALUE
REGION ADDRESS
REGION LENGTH
PROTOCOL INFORMATION
NEXT
124
READ REGION ADDRESS/LENGTH FROM BUFFER DESCRIPTOR
REGION DECRIPTOR
REGION ADDRESS
REGION LENGTH
128
NEXT

FIG. 4

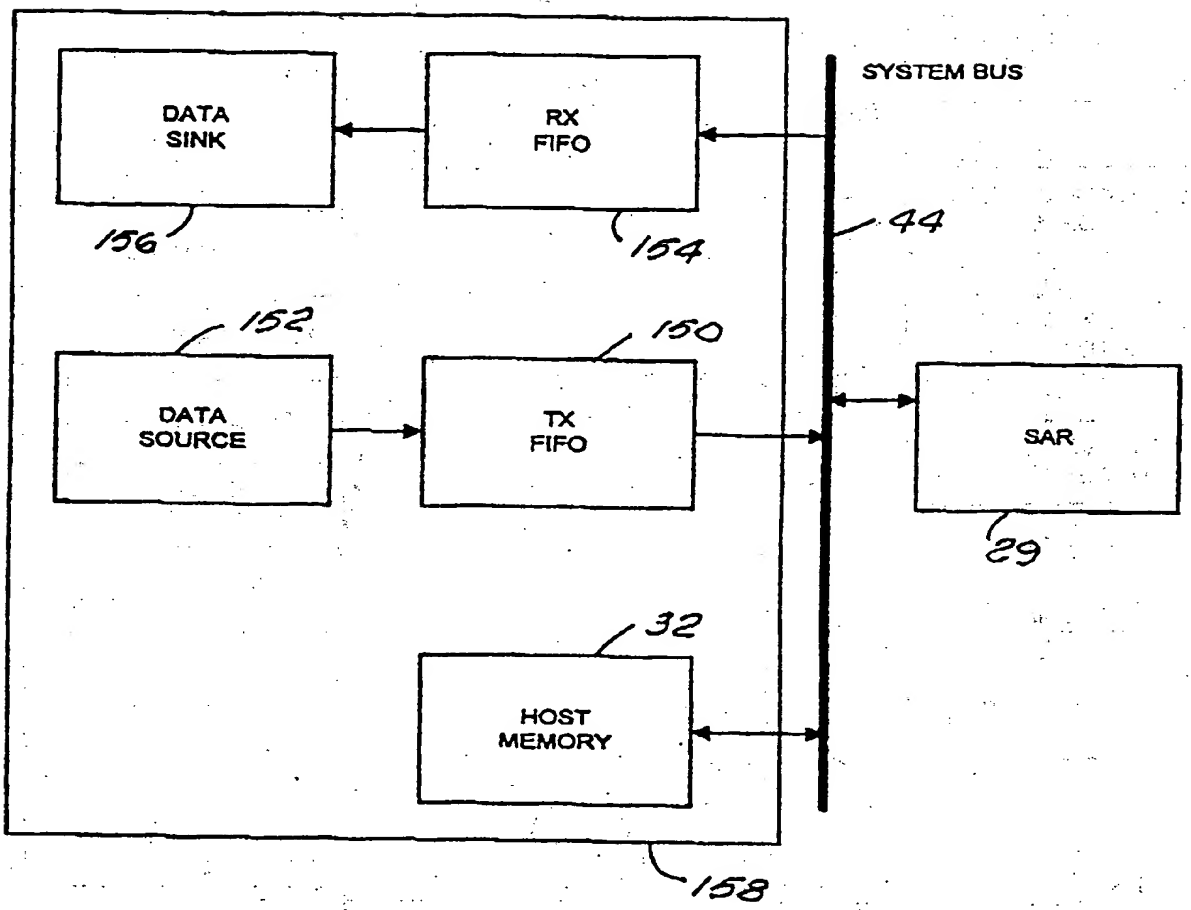

FIG. 5

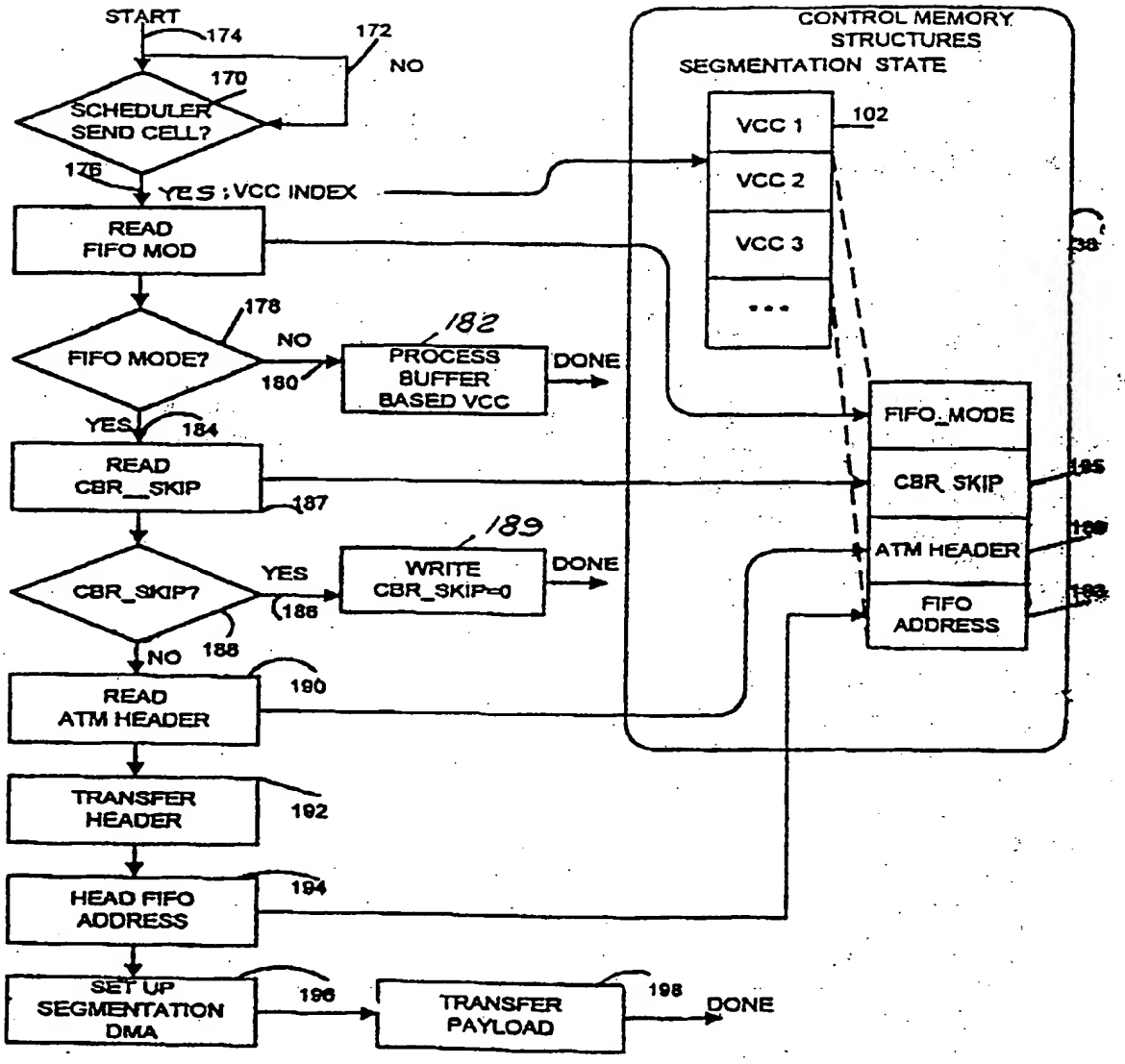
START
174
172
NO
170
SCHEDULER SEND CELL?
176
YES ; VCC INDEX
READ FIFO MOD
178
FIFO MODE?
NO
180
182
PROCESS BUFFER BASED VCC
DONE
YES
184
READ CBR_SKIP
187
189
CBR_SKIP?
YES
186
WRITE CBR_SKIP=0
DONE
NO
188
READ ATM HEADER
190
TRANSFER HEADER
192
HEAD FIFO ADDRESS
194
SET UP SEGMENTATION DMA
196
TRANSFER PAYLOAD
198
DONE
CONTROL MEMORY STRUCTURES
SEGMENTATION STATE
VCC 1
102
VCC 2
VCC 3
...
38
FIFO_MODE
CBR_SKIP
195
ATM HEADER
FIFO ADDRESS
193

FIG. 6

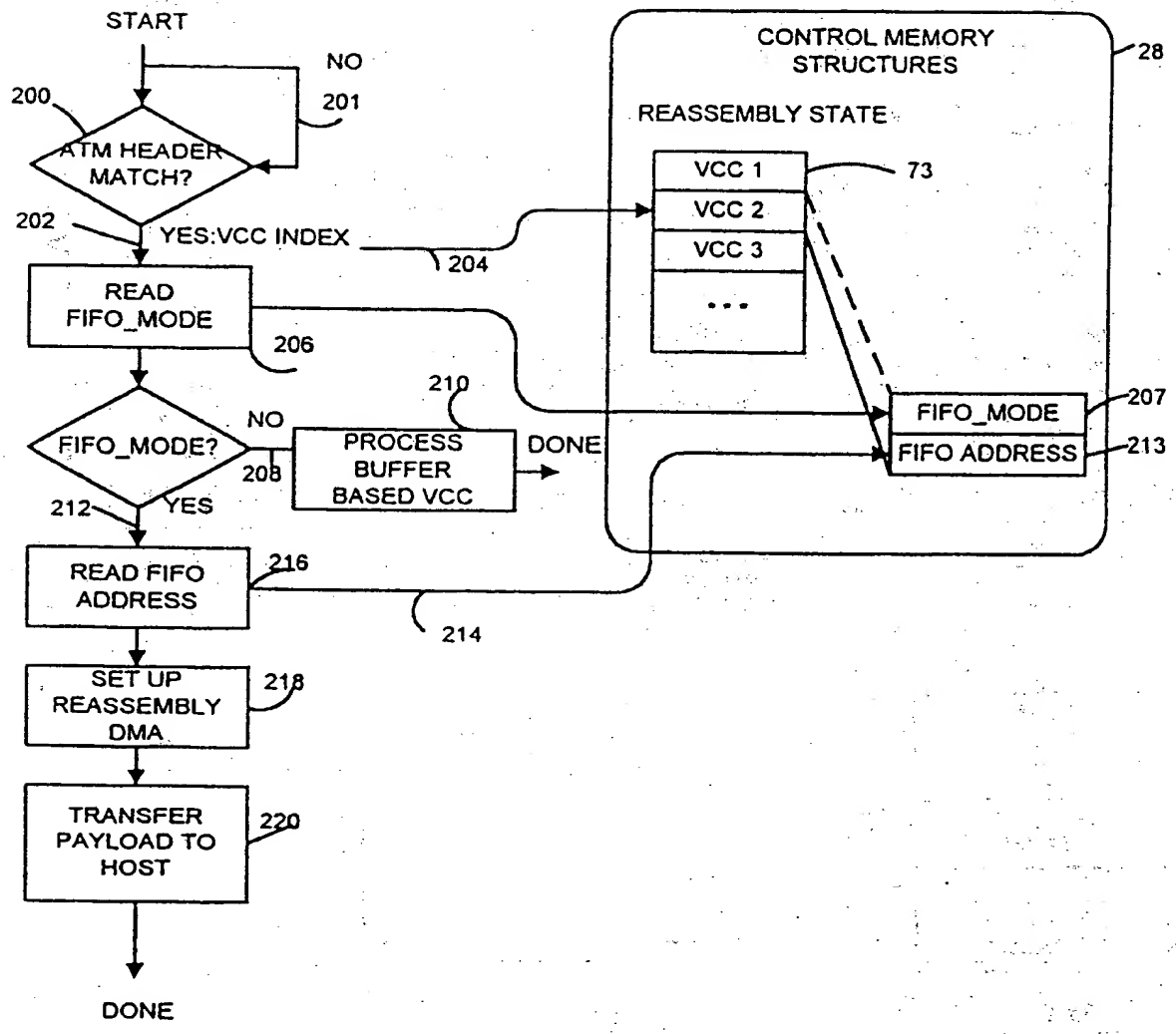

FIG. 7